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PIPELINED DELTA SIGMA MODULATOR ANALOG TO DIGITAL CONVERTER FOR SOC APPLICATIONS

Saiyu Ren, Ray Siferd, and Robert Blumgold

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AIR FORCE MATERIEL COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7320

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/S/

ROBERT M. BLUMGOLD
Electronic Engineer
Multi-Chip Integration Branch
AFRL/SNDI

/S/

ALAN J. TEWKSBURY, Chief
Multi-Chip Integration Branch
Aerospace Components Division
AFRL/SNDI

/S/

TODD CASTLE
Aerospace Components Division
Sensors Directorate
AFRL/SNDI

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Saiyu Ren and Ray Siferd (Wright State University)
Robert Blumgold (AFRL/SNDI)

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Systran Federal Corporation
4027 Colonel Glenn Highway
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Dayton, OH

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A two stage Pipelined Delta Sigma Modulator analog to digital converter is presented for broad band, high resolution System On a Chip (SOC) applications. Input bandwidth is 62.5 MHz and the sampling frequency of 1 GHz results in an oversampling ratio of 8, and a 12-bit resolution with a 50 MHz input.

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Pipelined Delta Sigma Modulator Analog to Digital Converter for SOC Applications

Saiyu Ren Ray Siferd
Department of Electrical Engineering
Wright State University, Dayton, OH

Robert Blumgold
Sensors Directorate, Air Force Research Laboratory
Wright Patterson AFB, OH

Abstract

A two stage Pipelined Delta Sigma Modulator ADC is presented for broad band, high resolution SOC applications. The unique architecture incorporates a first order delta sigma modulator in each stage and combines the most significant bits of the first stage with the second stage output to produce 11-13 bit resolution. The input bandwidth is 62.5 MHz and the sampling frequency of 1 GHz results in an over sampling ratio of 8 for the first order modulators. MATLAB simulations for the two stage ADC show 13-15 bit resolution. A transistor level design in 0.18um CMOS for the two stage ADC captured and simulated with Cadence show 12 bit resolution with a 50 MHz input.

1. Introduction

The analog to digital converter (ADC) has become a critical component for advanced telecommunication systems. The desire to move the analog to digital interface closer to the sensor has resulted in more stringent performance requirements for broad band, high resolution ADCs. A popular ADC architecture for broad band applications is the Nyquist Rate Pipelined ADC [1] [2]. The pipelined ADC achieves broad band operation together with good resolution by using several pipelined stages of low resolution flash ADCs. High resolution pipelined ADCs require highly accurate and precise matching for components such as DACs and analog buffers, delays, and subtract circuits. Delta Sigma Modulator ADCs reduce the requirements for highly accurate and matched components by incorporating over sampling and noise shaping [3]. Broad band operation requires low over sampling ratios, which then limits the resolution. Several techniques have been used to increase resolution of Delta Sigma Modulators with low over sampling rations. These techniques include increasing the order of the modulator to improve the noise shaping and using multi-bit quantization, or some combination of both. [3]. Higher order modulators introduce stability issues and multi-bit quantization introduces DAC nonlinearity problems. Another approach uses cascading of multi-bit feed forward modulators to achieve higher order noise shaping [4], but this approach has problems with DAC nonlinearity, component accuracy and limited sampling rate. This paper presents a unique Pipelined Delta Sigma Modulator (PDSM) ADC[5]. High resolution, broad band operation is achieved by pipelining two or more stages of first order modulators with multi-bit quantization. First order modulators eliminate stability problems and also help to facilitate high sampling ratios. A unique averaging technique is used for generating the analog error input signal to the second (and subsequent) stages, which mitigates the effect of DAC nonlinearities and component accuracy of key analog circuits such as track/hold and subtract. The next section summarizes some basic concepts and the operation of the PDSM ADC. Performance is then assessed using Matlab simulations and simulations of a transistor level design using 0.18um CMOS technology.

2. Two Stage Pipelined Delta Sigma Modulator (PDSM) ADC Architecture

The architecture for the two stage PDSM ADC is shown in Figure 1. As seen in Figure 1, the first stage of the PDSM ADC is a standard first order delta sigma modulator with a discrete integrator, multi-bit quantizer, and a two stage low pass filter. A four bit quantizer is used for this implementation and the clock frequency (fs) is 1 GHz. An input bandwidth of 62.5 MHz is selected, which results in an over sampling ratio (OSR) of 8. The four bit output of the quantizer is passed through two stages of low pass filtering. After filtering the digital output of the first stage is a 13 bit word. The 13 bit digital output is only accurate to 7-8 bits with an OSR of 8. The resolution of the first stage would increase with a higher OSR. Again referring to Figure 1, the input to the second stage is the difference between the analog input (after a clock delay) and the analog version of the output of the first stage quantizer.

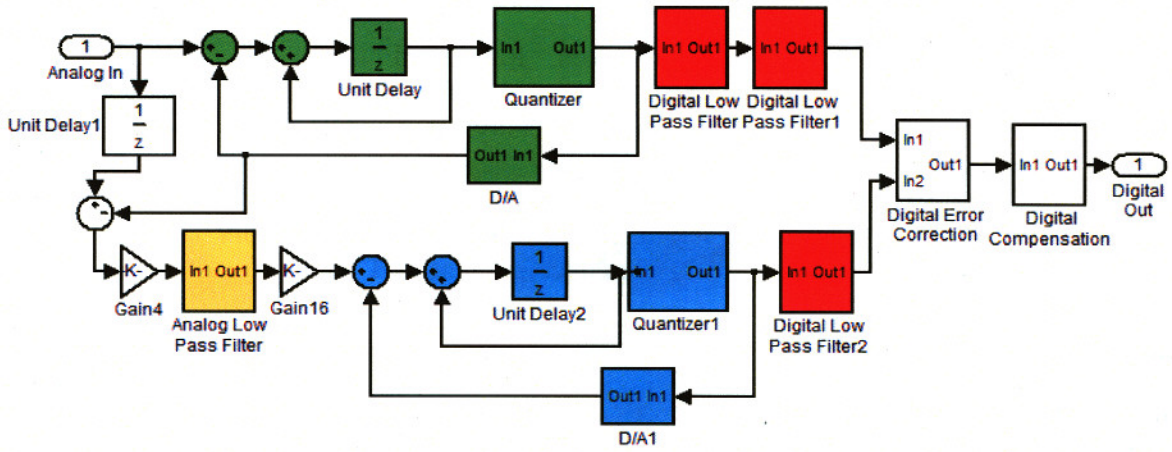

Figure 1
Two Stage PDSM ADC Architecture

This analog error signal is then put through an analog low pass filter that has the same sampled data transfer function as the digital low pass filters for stage one. A good candidate for both the digital and analog filters is a cascade of two averaging filters. The transfer function for each stage of the averaging filters is

$$T_{ave}(z) = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i}$$

Tave(z) has a Sinc function frequency response with a null at f=fs/M. For this application, choosing M=OSR=8 results in the null at 125 MHz, which is twice the band width. The magnitude of the in band signals are attenuated by the $(\text{Sinc})^2$ function and must be precisely offset by the compensation filter after combining the first and second stage digital outputs. After passing though the analog low pass filter, the high frequency components of the error signal are attenuated, leaving a predominantly low frequency error signal that is amplified so that the dynamic range is the same as the analog input signal. The filtered and amplified error signal is the input to the second stage first order modulator and digital low pass filter as seen in Figure 1. The digital output of the second stage digital filter (which is again a cascade of two Sinc averaging filters) is the digital version of the error signal. The digital word is 10 bits wide, but only accurate to 5-6 bits. The digital outputs of the first stage and second stage are combined with the proper weighting to obtain an output that should be accurate to 11-13 bits for a two stage PDSM ADC. As mentioned above the, compensation filter must precisely offset the in band attenuation due averaging filters. Note that both the first stage output and the second stage output is subjected to the same total filter transfer function of $(\text{Sinc})^4$. Some key features of the PDSM ADC architecture are:

- High resolution and broad band operation with low OSR
- Accuracy requirements for track and hold circuits and analog subtract circuits are mitigated by the analog averaging of the error signal
- Over all component matching and accuracy requirements are reduced by the over sampling delta sigma configuration
- Nonlinearity of the first stage DAC/quantizer is included in the error signal and is cancelled when the second stage output is combined with first stage
- Pipeline operation is based on first stage generating 6-7 most significant bits and second stage generating 5-6 lease significant bits using first order delta sigma modulators.
- PDSM architecture differs from MASH or feed forward architectures that seek to obtain higher order delta sigma operation. First order modulators used by PDSM ADC facilitate high sampling rates.

3. Matlab Simulation Results

The PDSM ADC two stage architecture was captured using the MATLAB/SIMULINK simulator to verify the feasibility of obtaining the high resolution/broad bandwidth performance. The delta sigma modulators are implemented with 4 bit quantizers and all analog mathematical functions are ideal. The cascaded averaging filters are of length M=8 and are realized by using the appropriate transfer function in the z domain. The sampling frequency is 1 GHz and the analog input signal is in the frequency band of 0 to 62.5

MHz.. The Fast Fourier Transform (FFT) of the output signal is shown in Figure 2 below for an input of 50 MHz.

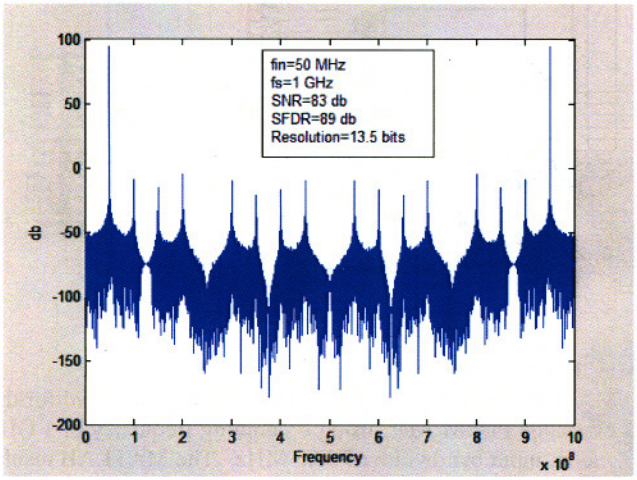

Figure 2
Matlab FFT Results for 50 MHz Input

The FFT results indicate that the two stage PDSM ADC has a resolution of 13.5 effective bits for a 50 MHz input. The Spur Free Dynamic Range (SFDR)=89 db for 50 MHz input. The FFT of the output signal for a 10 MHz input and a 25 MHz are shown in Figure 3 and 4 below. For the 10 MHz and 25 MHz inputs, the resolution is 15 effective bits and the SFDR is 106 db.

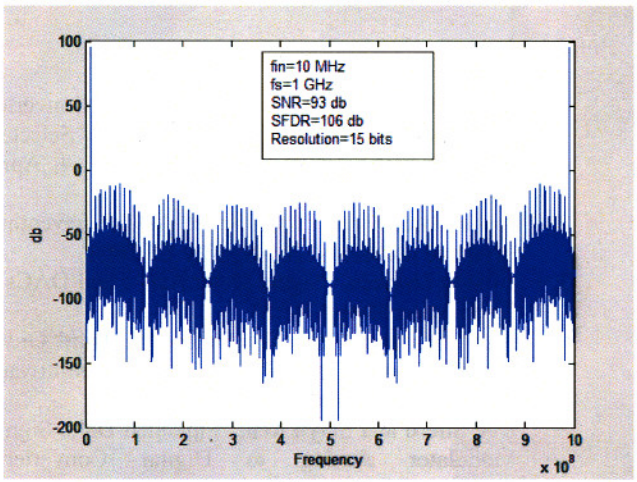

Figure 3
Matlab FFT Results for 10 MHz Input

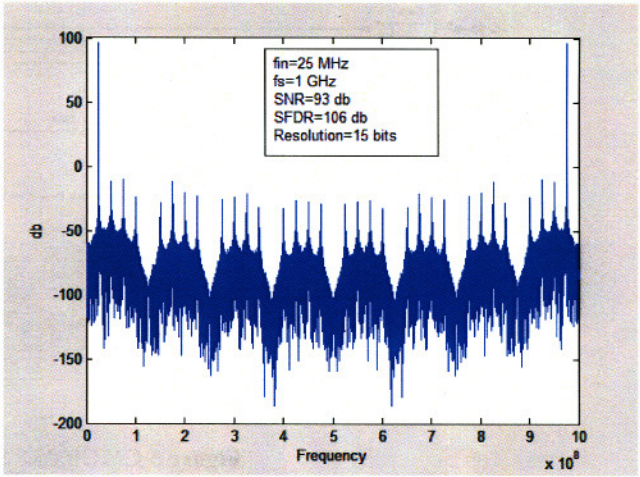

Figure 4
Matlab FFT Results for 25 MHz Input

4. PDSM ADC Performance of 0.18um CMOS Design

The two stage PDSM ADC was designed and a transistor level circuit captured using CMOS 0.18um technology. Figure 5 depicts the design as captured using the Cadence Analog Design Environment. The design incorporates a direct form integrator, which has performance advantages over a traditional switched capacitor (SC) or continuous time analog integration (CTAI) implementations, particularly for broadband applications with high sampling rates and relatively low over-sampling ratios [6]. The direct form integrator also can be used over a wide range of clock frequencies. All components, including track/hold and analog and digital filter can be clocked up to 1.2 GHz. The detailed schematics of the PDSM ADC design are not presented for lack of space. Each modulator has about 1000 transistors and consumes approximately 75 mil-watts of power when clocked at 1 GHz. The dynamic range of the input is 0.9 volt peak to peak for a 1.8 volt power supply. The 0.18 um CMOS version of the PDSM Pass ADC was simulated using the Cadence Analog Design Environment. The output data was captured and an FFT of the weighted sum of the output was performed using the Cadence tools. The input for this case was a sine wave with amplitude 0.4 volts and a frequency of 50 MHz. The clock is distributed throughout the PDSM ADC using a standard tree structure with buffers, so the simulation results include the effect of clock jitter.

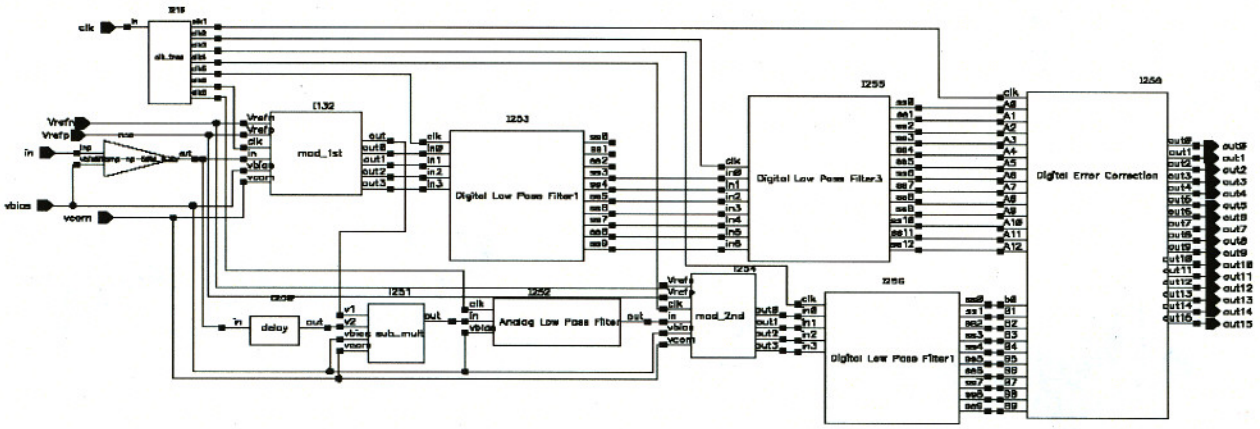

Figure 5 CMOS 0.18um Design For the PDSM ADC

The FFT results based on the weighted sum of the outputs are shown in Figure 6 for an input of 50 MHz. The simulation time was 2.0 microseconds, which took two weeks to complete. The signal to noise ration for a 62.5 MHz bandwidth was calculated based on the FFT and found to be about 76 db. This corresponds to about 12 bits of resolution. The SFDR is 78 db based on the highest spur at 61.5 MHz. The resolution of the FFT is constrained by the time length of the simulation, which as mentioned above is 2 u-seconds.

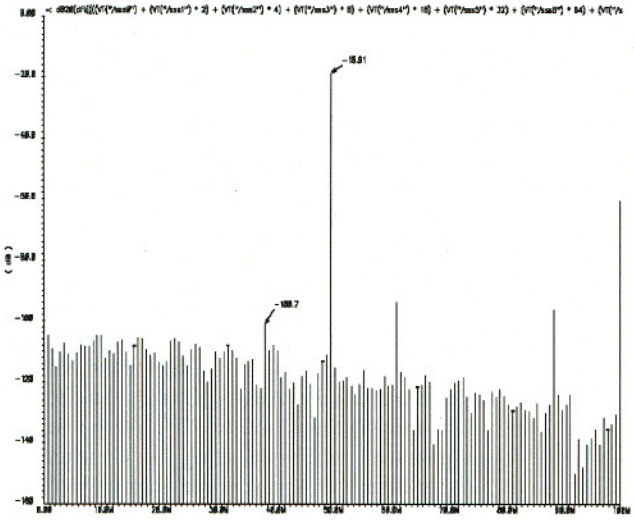

Figure 6 FFT Results for 0.18um CMOS Design

5. Conclusions

A unique architecture is presented for a high resolution, broad band ADC. The two stage PDSM ADC combines the features of over sampling delta sigma modulator ADCs with pipelined ADCs. The result is high resolution and broad band operation using first order modulators and low over sampling ratios. The architecture has features which relax the requirements for component accuracy and matching. MATLAB simulation and FFT results were presented for the two stage PDSM ADC using s sampling frequency of 1 GHz and an input bandwidth of 62.5 MHz. The MATLAB results support 13-15 bit resolution over the 62.5 MHz bandwidth. A transistor level 0.18um CMOS version of the design was captured using Cadence design tools with modulators and other components that can be clocked at 1 GHz. The FFT results, based on simulations of the CMOS 0.18um design, show 12 bit resolution with a 50 MHz input. These results support the practicality of using the PDSM ADC for SOC applications where there is a need for high resolution and broad band operation. Current efforts are being focused on capturing layouts for the two stage PDSM ADC for fabrication in 0.18um technology.

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